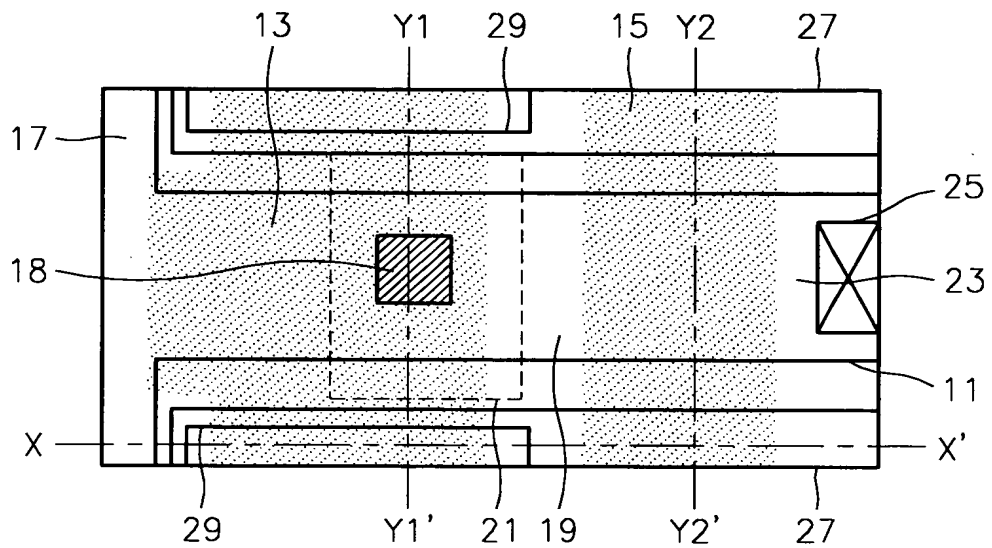
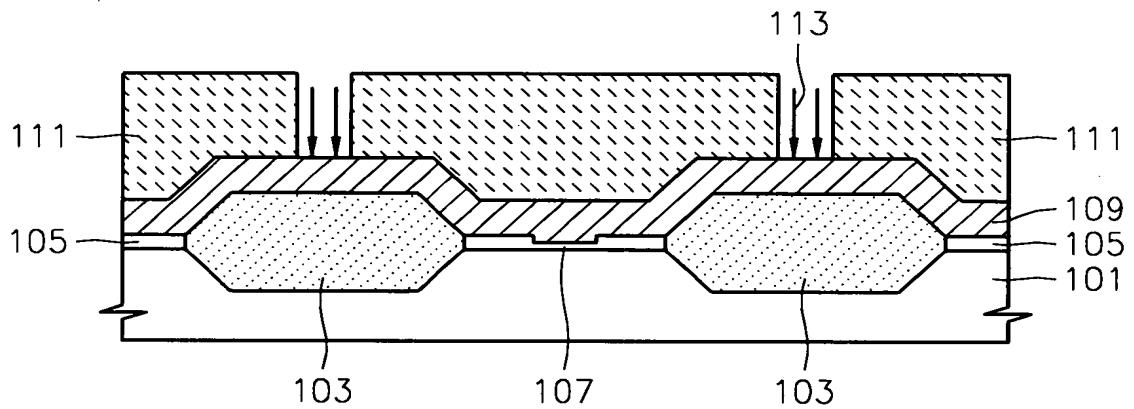


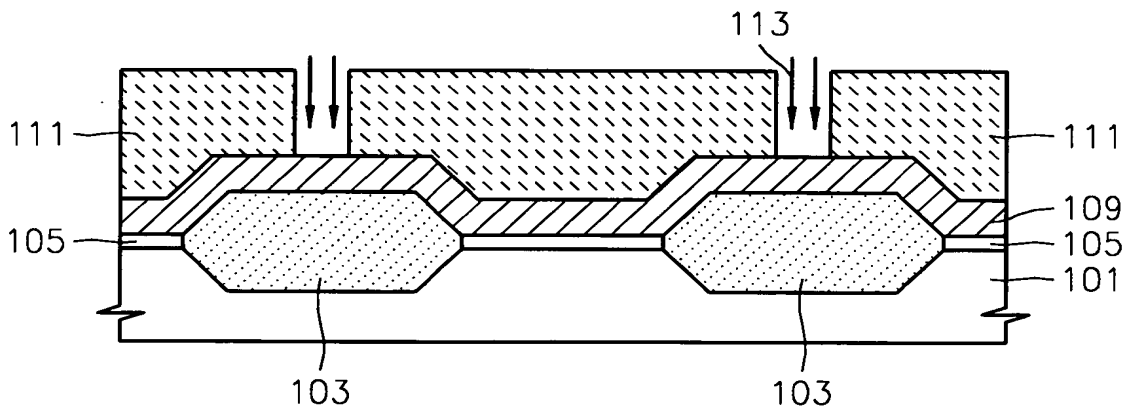
**FIG. 1 (PRIOR ART)**



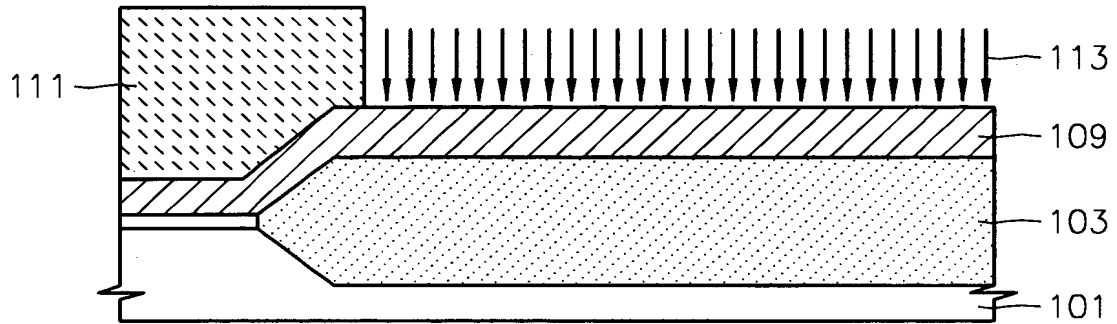
**FIG. 2A (PRIOR ART)**



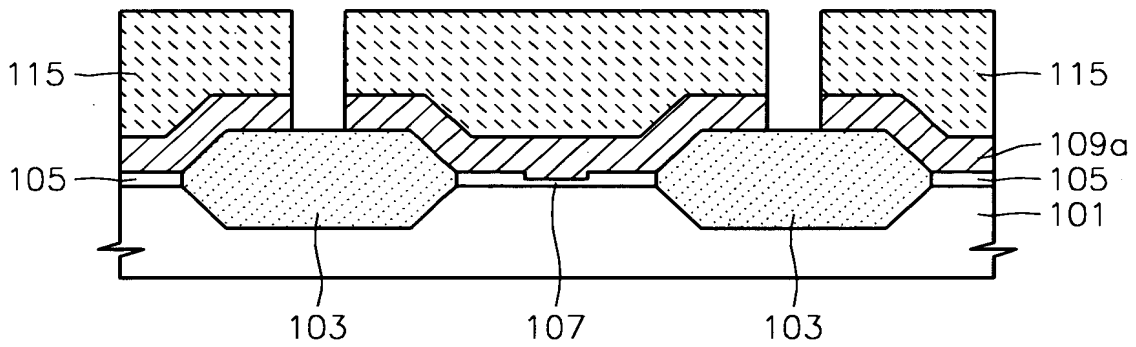
**FIG. 2B (PRIOR ART)**



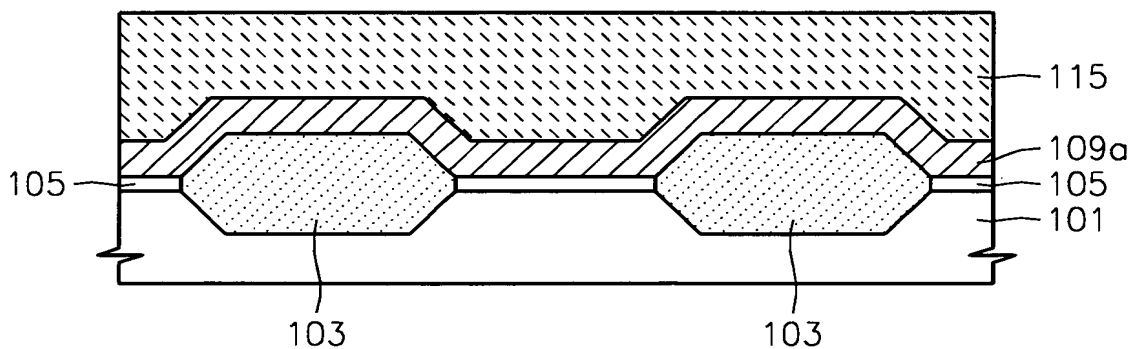
**FIG. 2C (PRIOR ART)**



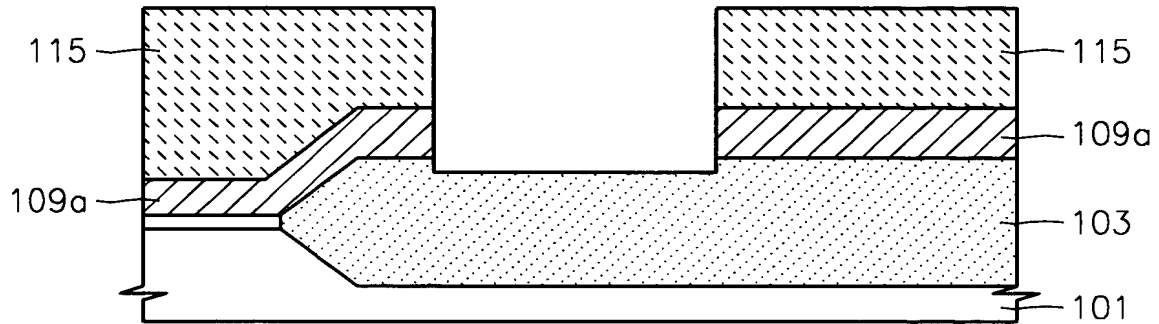
**FIG. 3A (PRIOR ART)**



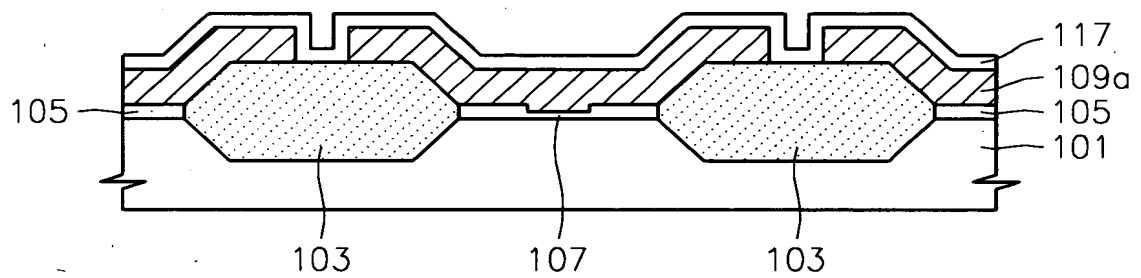
**FIG. 3B (PRIOR ART)**



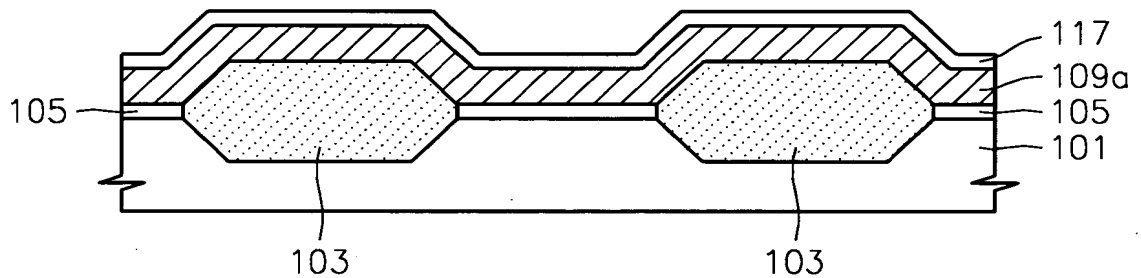
**FIG. 3C (PRIOR ART)**



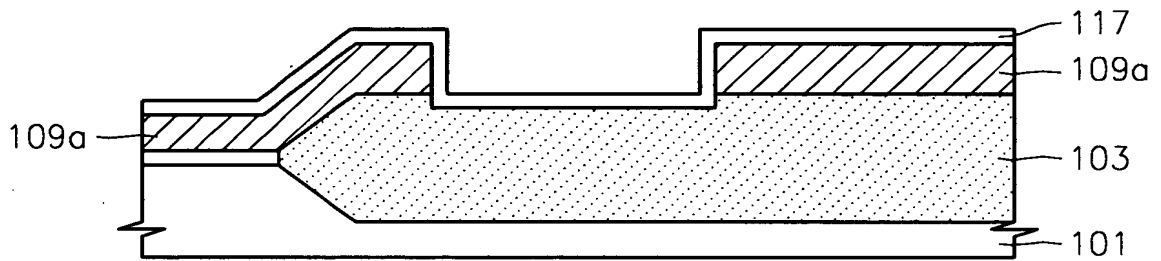
**FIG. 4A (PRIOR ART)**



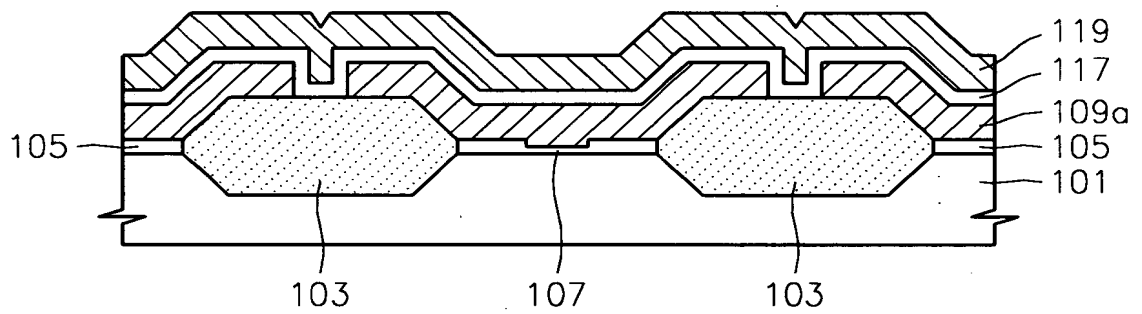
**FIG. 4B (PRIOR ART)**



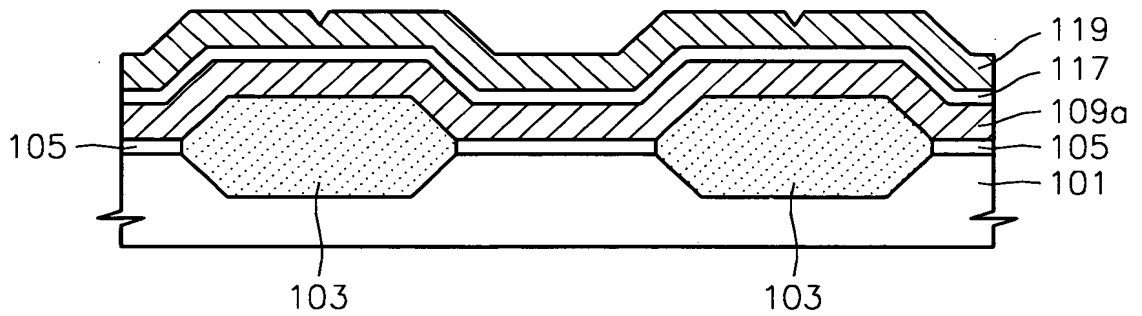
**FIG. 4C (PRIOR ART)**



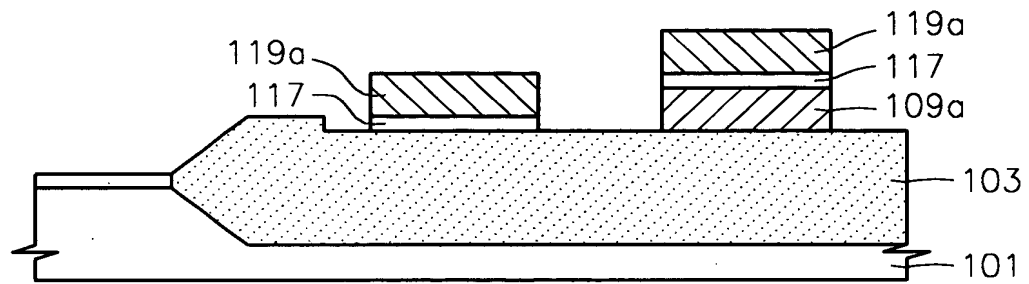
**FIG. 5A (PRIOR ART)**



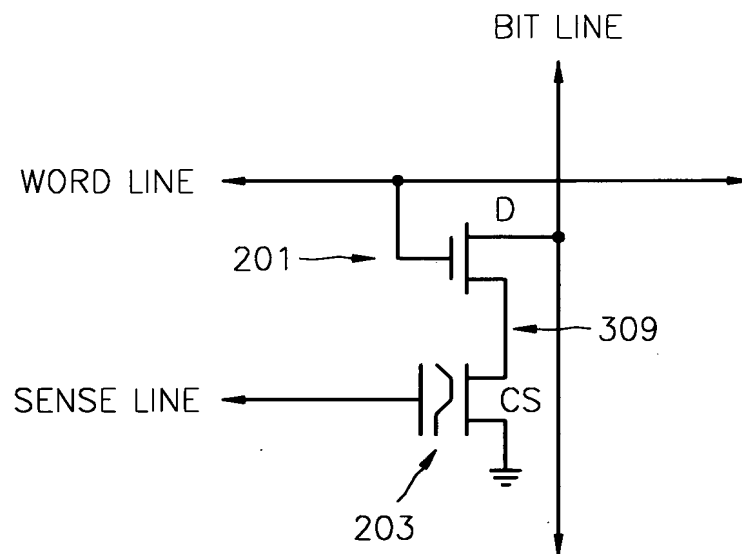
**FIG. 5B (PRIOR ART)**



**FIG. 5C (PRIOR ART)**



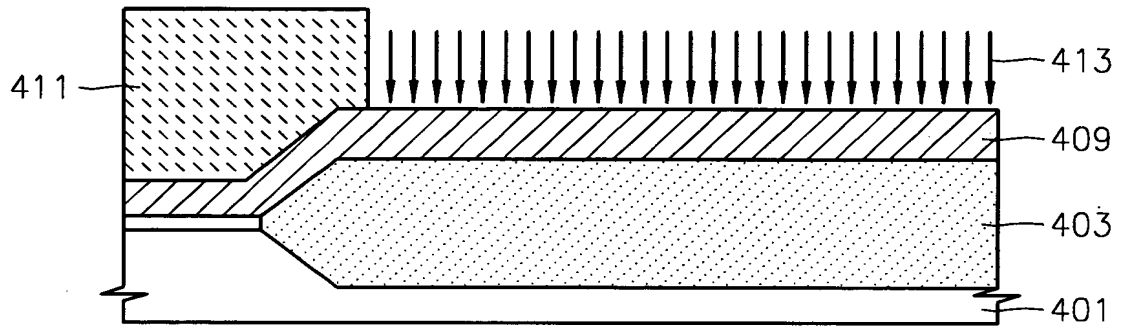
**FIG. 6**



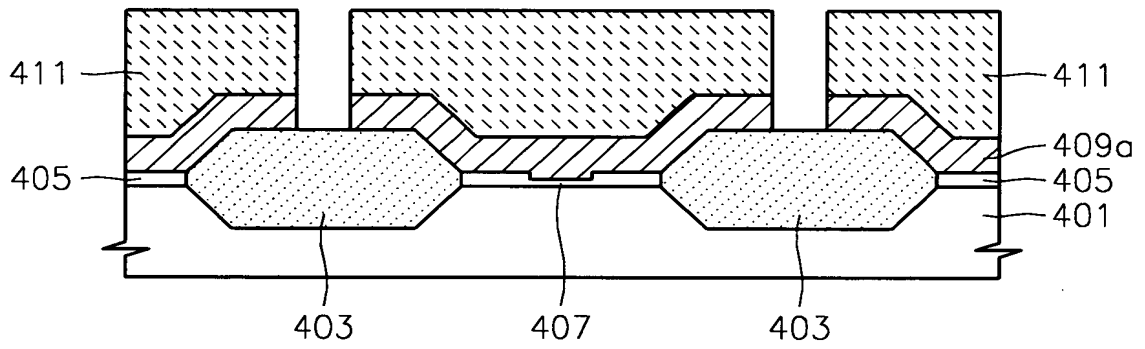
[illegible]

A cross-sectional view of a semiconductor device. The device features a central channel region (403) and two side regions (405). The channel region is defined by a central layer (407) and is flanked by side regions (405). The side regions are separated from the channel by a thin layer (409). The device is mounted on a substrate (401). The top surface is covered by a layer (411). Arrows (413) indicate a process step, likely etching, being applied to the top surface of the side regions.

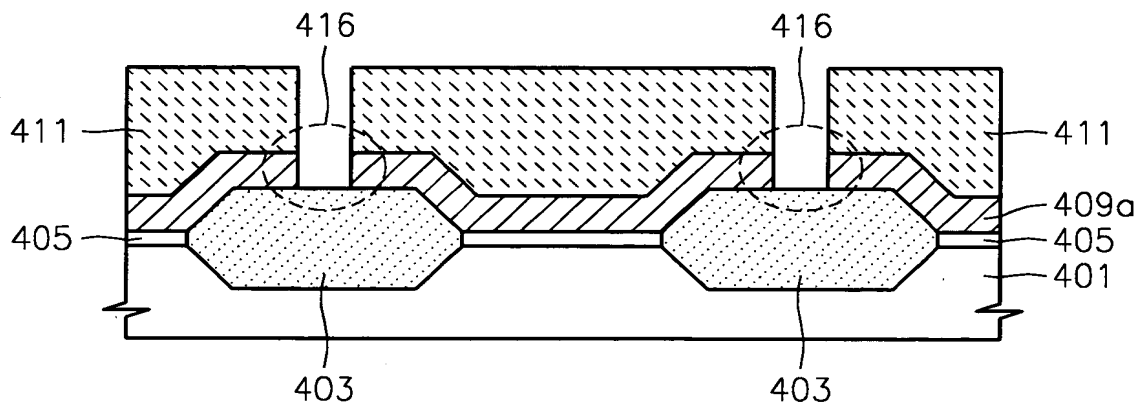
**FIG. 8C**



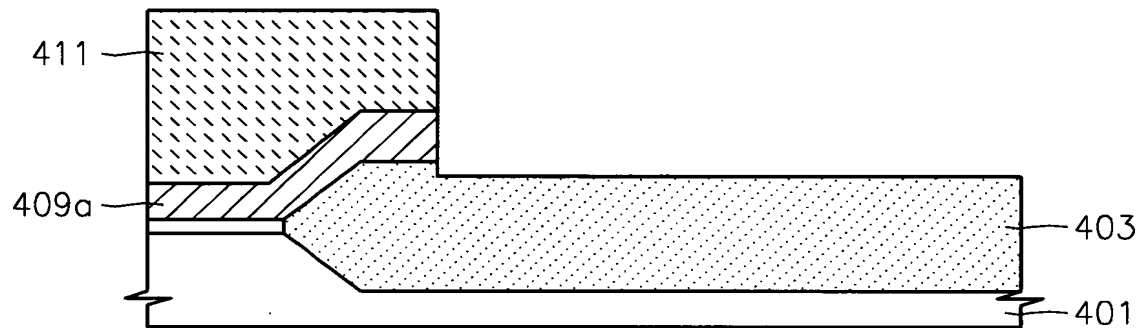
**FIG. 9A**



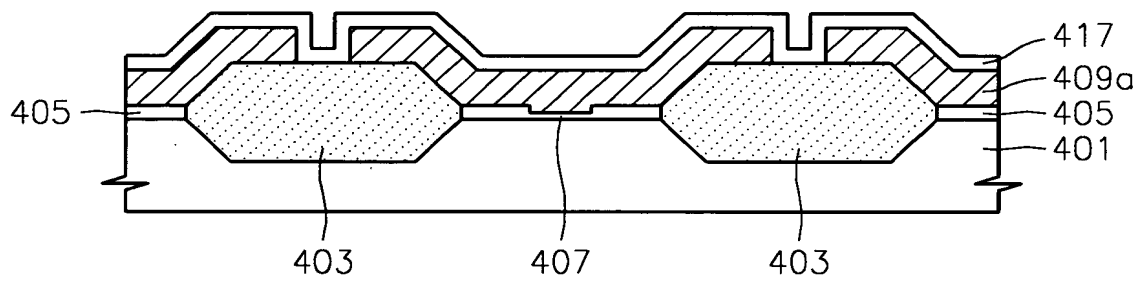
**FIG. 9B**



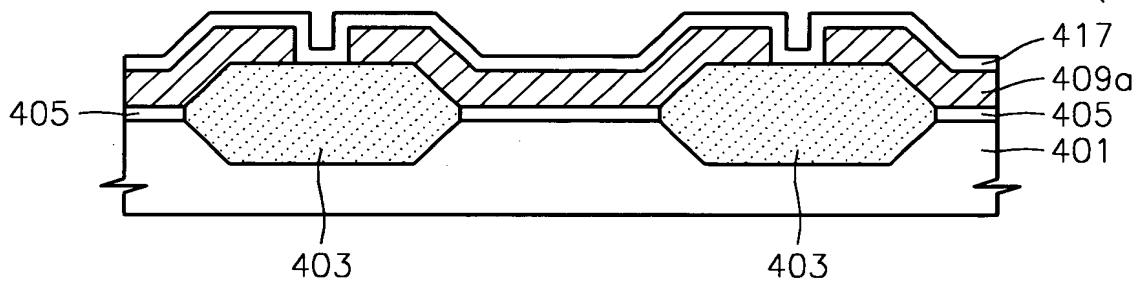
**FIG. 9C**



**FIG. 10A**

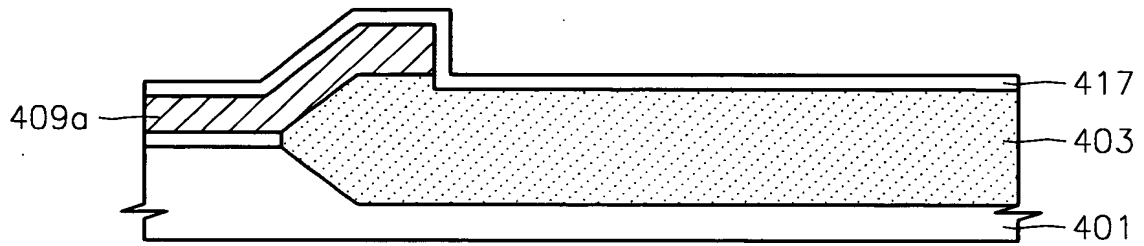


**FIG. 10B**

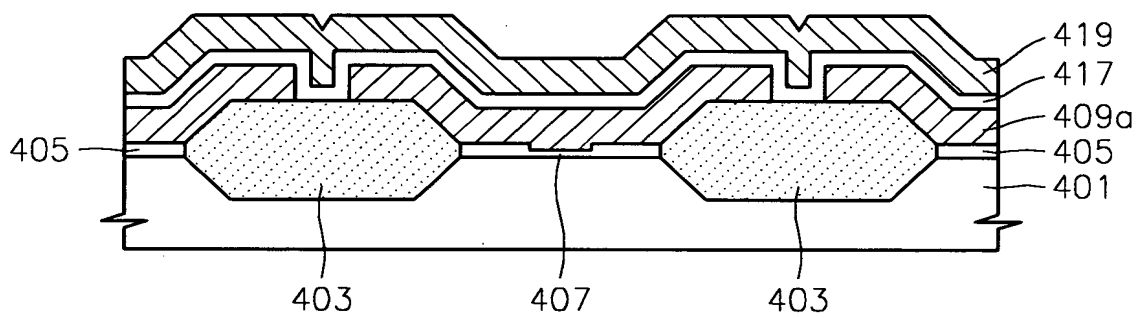




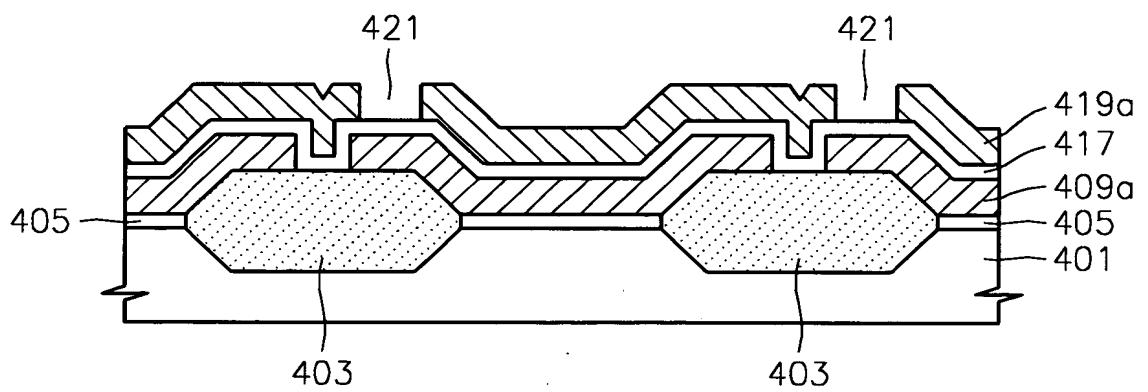
**FIG. 10C**



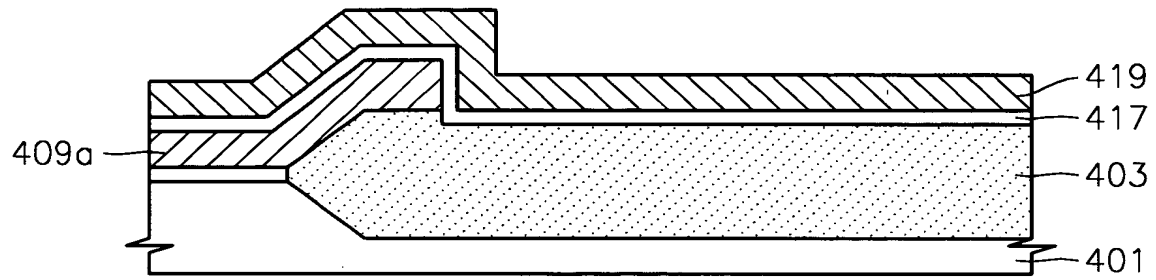
**FIG. 11A**



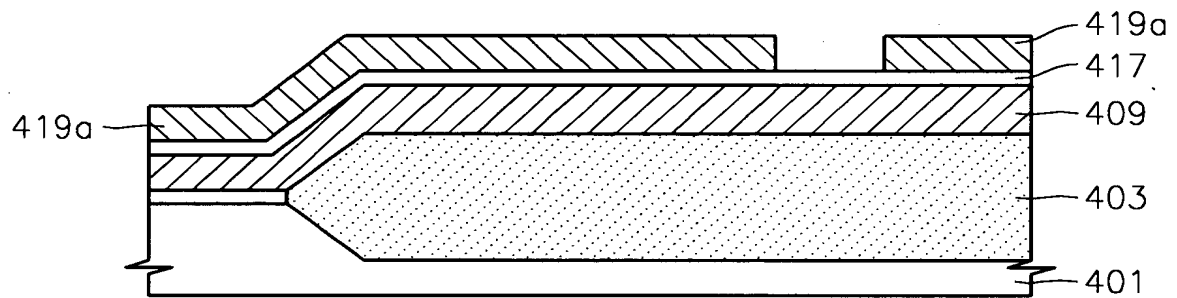
**FIG. 11B**



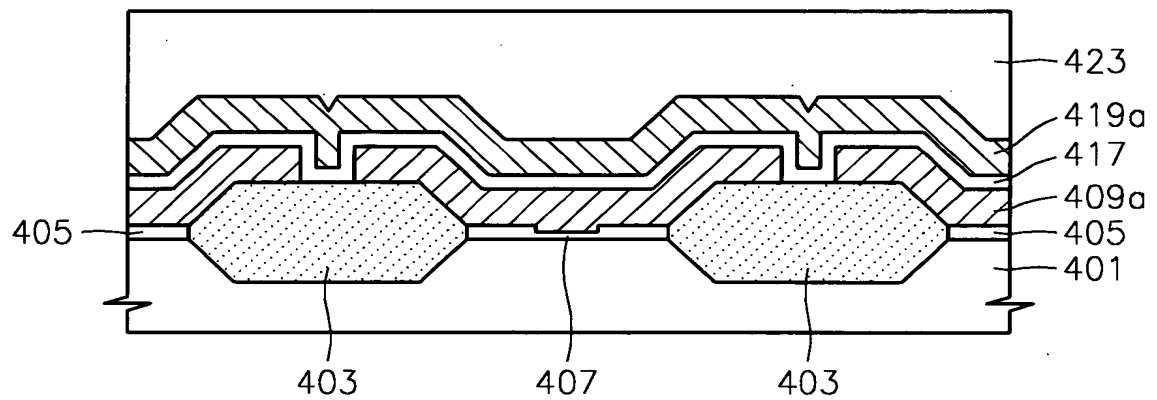
**FIG. 11C**



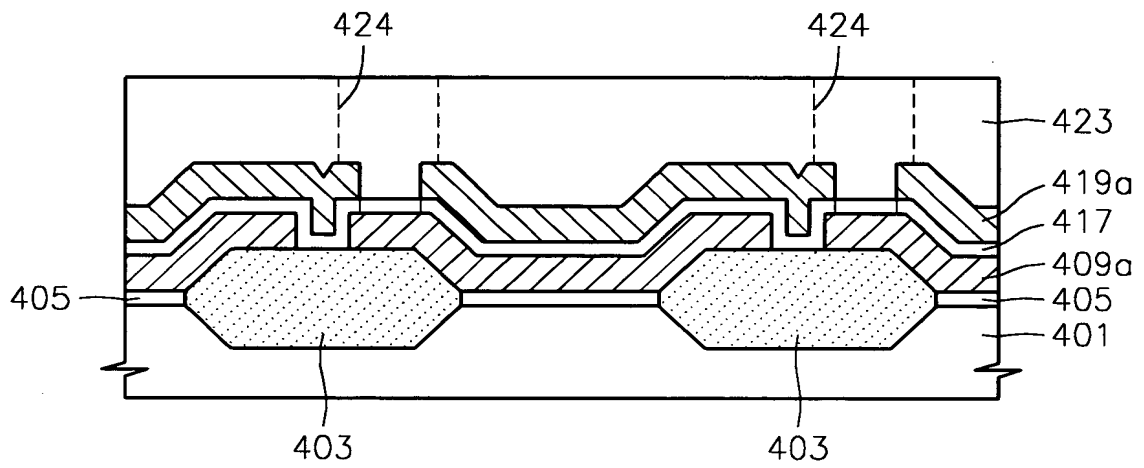
**FIG. 11D**



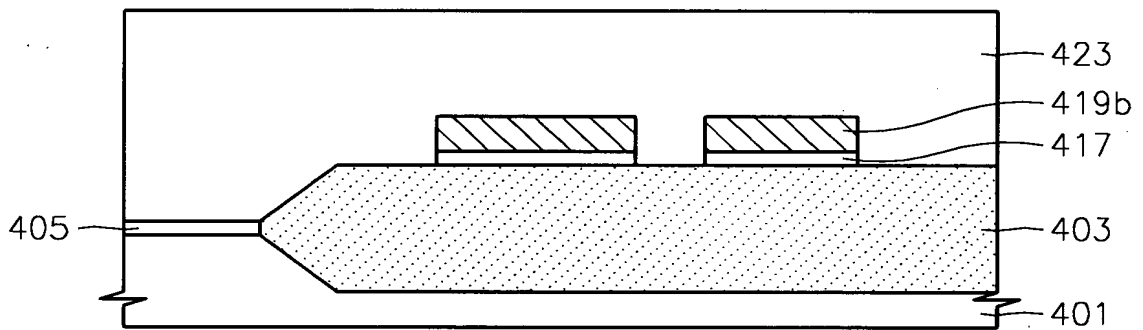
**FIG. 12A**



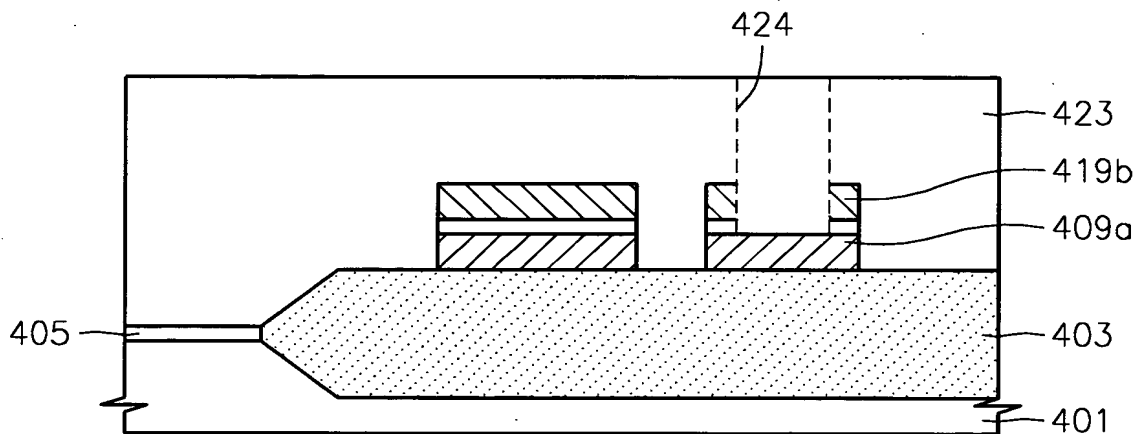
**FIG. 12B**



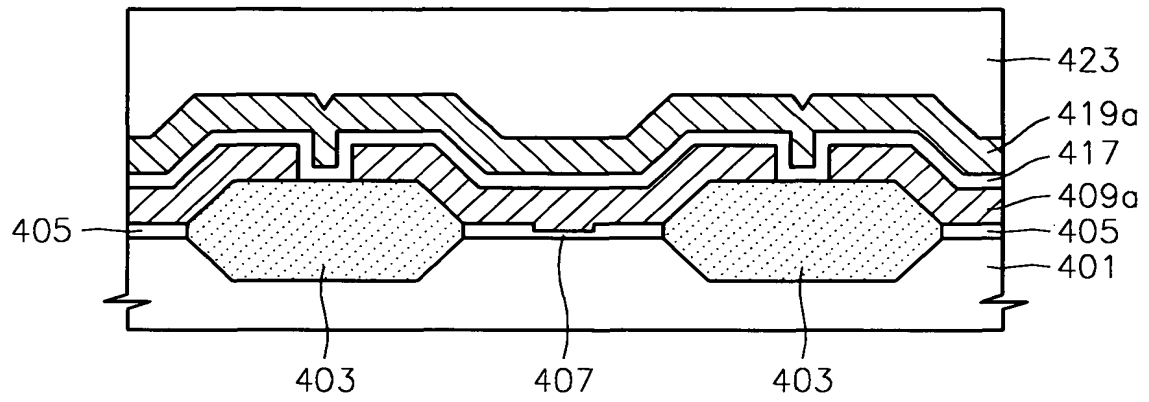
**FIG. 12C**



**FIG. 12D**



**FIG. 13A**



**FIG. 13B**

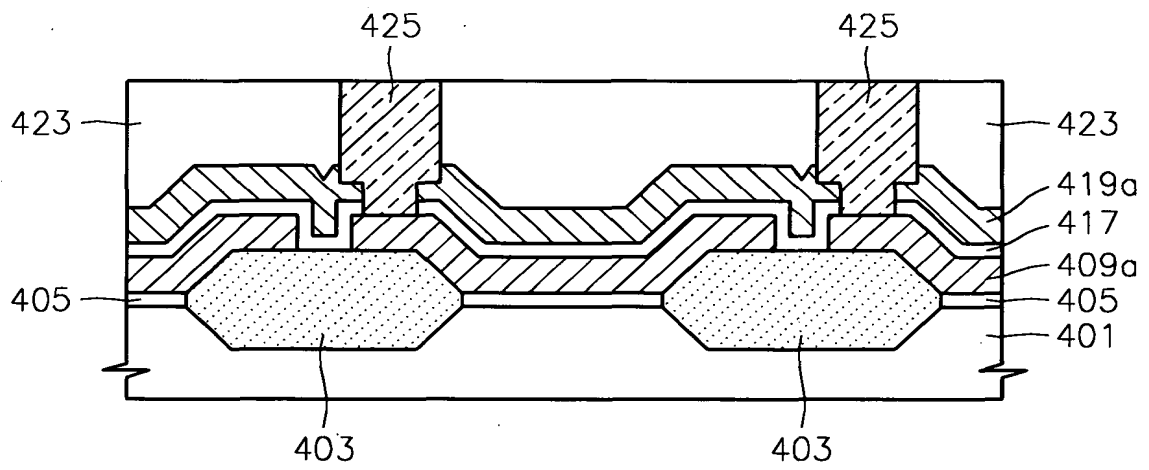


FIG. 13C

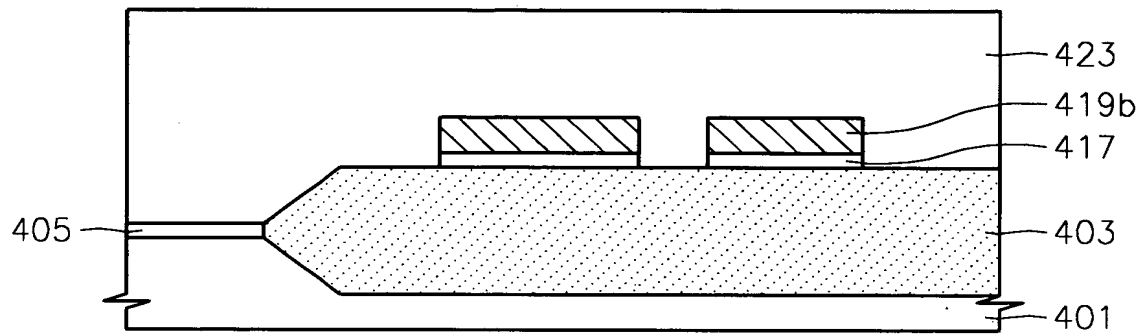


FIG. 13d

